EE 210: Digital Logic & Computer Systems

Term: Fall 2026
Credits: 4.0
Lecture Times & Location: Monday, Wednesday, Friday 8:00–8:50 a.m., Rowan Engineering Center 110
Laboratory Time & Location: Tuesday 8:00–10:50 a.m., Rowan Engineering Center 150
Modality: In-Person Lecture and Laboratory

Instructor Information

- **Instructor:** Dr. Tessa Becker (Associate Professor of Electrical & Computer Engineering)
- **Email:** tbecker@university.alkimi.ai
- **Office:** Rowan Engineering Center 214
- **Office Hours:**
  - Monday & Friday: 9:30–11:00 a.m. (In person, Rowan Engineering Center 214)
  - Wednesday: 4:00–5:00 p.m. (Virtual via Zoom; link posted in Canvas)
  - Also available by appointment.

Course Description

Number systems, Boolean algebra, combinational and sequential logic, finite state machines, and hardware description languages, with a weekly three-hour laboratory using FPGA boards. EE 210 provides a rigorous introduction to digital systems design, spanning Boolean algebra, combinational logic networks, synchronous sequential circuits, and modern hardware description languages. Students analyze and synthesize digital circuits using SystemVerilog, simulate designs using industry-standard EDA tools, and implement digital hardware on field-programmable gate array (FPGA) development boards. The course connects foundational gate-level logic with modular digital architectures including arithmetic logic units, finite state machines, and register files.

Prerequisites

CS 150.

Measurable Student Learning Outcomes

Upon successful completion of EE 210, students will be able to:

1. **Analyze and Minimize Boolean Logic:** Apply Boolean algebra theorems, Karnaugh maps, and algebraic factorization to minimize combinational logic functions and design optimal two-level and multi-level circuits.
2. **Design Combinational Subsystems:** Construct MSI combinational modules including multiplexers, decoders, priority encoders, comparators, and arithmetic circuits such as carry-lookahead adders and ALUs.
3. **Synthesize Synchronous State Machines:** Design, optimize, and encode Moore and Mealy finite state machines, deriving state transition diagrams, excitation tables, and next-state logic.

4. **Model Hardware with SystemVerilog:** Author synthesizable SystemVerilog models for combinational and sequential modules, write self-checking testbenches, and verify timing and functional correctness via simulation.
5. **Implement Digital Systems on FPGAs:** Program, test, and debug digital logic systems on physical FPGA development boards using switches, buttons, seven-segment displays, and serial communication interfaces.

Required Course Materials & Approximate Costs

1. **Harris, David, and Sarah L. Harris. *Digital Design and Computer Architecture: RISC-V Edition*. Morgan Kaufmann, 2021.** Approx. $75 digital rental ($95 purchase; reserve copies available in Alkimi Library).
2. **FPGA Development Board (Digilent Basys 3 Artix-7) and EDA synthesis software (Vivado ML Standard).** Provided in laboratory Rowan Engineering Center 150; free software download for student laptops.
3. **Total estimated cost:** Approx. $0 (library reserve & lab equipment) to $75 (textbook rental).

Generative AI Policy (AI Level 2: AI Permitted with Disclosure for Specified Tasks)

In accordance with Alkimi University Academic Policies (Student Handbook §5.8), EE 210 operates under **AI Level 2**.

- **What is permitted:** Students may consult AI tools to clarify SystemVerilog syntax, understand simulator compiler error diagnostics, and learn standard testbench assertion patterns.
- **What is prohibited:** Generative AI must not be used to author complete SystemVerilog modules for graded lab assignments, generate state machine transition logic for project deliverables, or complete examination questions. All hardware designs must be synthesized and tested independently.
- **Disclosure:** Whenever AI tools are consulted to resolve HDL syntax or understand simulation anomalies, students must document the interaction in their lab notebook with the exact prompt and describe how the design was physically verified on the FPGA board.

Grading Components and Weights

- **Weekly Problem Sets:** 10% (Due Wednesdays at 11:59 p.m. in Canvas (weeks 2–14; lowest dropped))
- **Laboratory Experiments & FPGA Checkoffs:** 25% (Completed during Tuesday lab sessions with checkoffs and lab reports due Sundays at 11:59 p.m. (lowest dropped))
- **FPGA Digital System Design Project:** 15% (Due Friday, November 20 at 11:59 p.m.)
- **Midterm Exam 1 (Combinational Logic & HDLs):** 15% (In class, Friday, October 2)
- **Midterm Exam 2 (Sequential Logic & State Machines):** 15% (In class, Friday, November 6)
- **Comprehensive Final Examination:** 20% (Monday, December 14, 2026, 8:00–10:00 a.m.)

Grading Scale (Alkimi University Standard)

- **A:** 93–100% | **A-:** 90–92%
- **B+:** 87–89% | **B:** 83–86% | **B-:** 80–82%
- **C+:** 77–79% | **C:** 73–76% | **C-:** 70–72%
- **D+:** 67–69% | **D:** 60–66% | **F:** Below 60%
- **Extra credit:** No extra credit assignments are offered in EE 210.

Course Schedule (Fall 2026)

Week	Dates	Topics & Readings	Laboratory	Assignments & Deadlines
Week 1	Aug 26, 28	**Number Systems and Digital Abstractions:** Analog vs. digital signals, binary, octal,	*No lab meetings this week.*	*First day of classes: Wed Aug 26.*

Week	Dates	Topics & Readings	Laboratory	Assignments & Deadlines
		hexadecimal, two's complement integer arithmetic, overflow detection, and logic voltage levels. *Reading: Harris & Harris Ch. 1.1–1.4*		
Week 2	Aug 31–Sep 4	**Boolean Algebra and Combinational Logic Gates:** Boolean axioms, De Morgan's laws, truth tables, SOP and POS canonical forms, NAND/NOR universal logic gates, and gate propagation delay. *Reading: Harris & Harris Ch. 1.5–1.7, 2.1–2.3*	Lab 1: Breadboarding Basic CMOS Logic Gates and Truth Tables	*Wed Sep 2: Add/section change deadline.*
Week 3	Sep 9, 11	**Logic Minimization and Karnaugh Maps:** Two-, three-, and four-variable Karnaugh maps, prime implicants, don't-care conditions, hazard conditions, and glitch-free combinational logic design. *Reading: Harris & Harris Ch. 2.4–2.7*	Lab 2: Combinational Logic Simplification and SSI Circuit Prototyping	*Mon Sep 7: Labor Day (no classes). Wed Sep 9: Census date (last day to drop without a W).*
Week 4	Sep 14–18	**Hardware Description Languages: SystemVerilog:** HDL design flow, structural vs. behavioral modeling, continuous assignment, wire vs. logic types, and writing basic simulation testbenches. *Reading: Harris & Harris Ch. 4.1–4.4*	Lab 3: SystemVerilog Modeling, Simulation, and FPGA Toolflow	—
Week 5	Sep 21–25	**Combinational Building Blocks:** Multiplexers, decoders, encoders, priority encoders, code converters, seven-segment display drivers, and tri-state buffers. *Reading: Harris & Harris Ch. 2.8, 4.5*	Lab 4: Multi-bit Multiplexers, Seven-Segment Display Decoders on FPGA	—
Week 6	Sep 28–Oct 2	**Arithmetic Circuits and Midterm Exam 1:** Half adders, full adders, ripple-carry adders, carry-lookahead adders, ALUs, and administration of Midterm Exam 1 in Friday lecture. *Reading: Harris & Harris Ch. 5.1–5.3*	Lab 5: Design and Simulation of an 8-bit Arithmetic Logic Unit	**Midterm Exam 1 (Combinational Logic & HDLs) (in class).**
Week 7	Oct 5–9	**Sequential Logic Fundamentals:** SR latches, D latches, edge-triggered D flip-flops, register structures, setup and hold times, clock-to-Q delays, and timing violations. *Reading: Harris & Harris Ch. 3.1–3.3*	Lab 6: Latches, D Flip-Flops, Glitches, and Metastability	—
Week 8	Oct 14, 16	**Synchronous Sequential Circuit Analysis:** Synchronous design methodology, clock skew, dynamic timing analysis, maximum clock frequency calculations, and metastable state resolution. *Reading: Harris & Harris Ch. 3.4–3.5*	*No lab meetings this week (holiday).*	*Oct 12–Oct 13: Fall break (no classes). Fri Oct 16: Midterm grades due.*
Week 9	Oct 19–23	**Finite State Machines: Moore and Mealy Models:** State diagrams, state tables, state assignment and encoding (binary, one-hot, Gray code), next-state logic, and output logic synthesis. *Reading: Harris & Harris Ch. 3.4, 4.6*	Lab 7: SystemVerilog Finite State Machine Design: Traffic Light Controller	—
Week 10	Oct 26–30	**Sequential Building Blocks: Counters and Registers:** Synchronous and asynchronous counters, up/down counters, shift registers, ring counters, linear feedback shift registers (LFSR), and button debouncers. *Reading: Harris & Harris Ch. 5.4–5.5*	Lab 8: Synchronous Counters, Shift Registers, and Debouncing Logic	—
Week 11	Nov 2–6	**Memory Arrays and Midterm Exam 2:** ROM, static RAM (SRAM), dynamic RAM (DRAM), multi-port register files, and administration of	Lab 9: Memory Modeling: Register Files and Dual-Port SRAM	*Fri Nov 6: Last day to withdraw (W) or elect Pass/No Pass.* **Midterm Exam 2 (Sequential**

Week	Dates	Topics & Readings	Laboratory	Assignments & Deadlines
		Midterm Exam 2 in Friday lecture. *Reading: Harris & Harris Ch. 5.6*		**Logic & State Machines) (in class).**
Week 12	Nov 9–13	**Timing Analysis and Clock Synchronization:** Clock domain crossing, two-flop synchronizers, FIFO buffer synchronization, and static timing analysis reports in FPGA synthesis. *Reading: Harris & Harris Ch. 3.5, 4.8*	Lab 10: Clock Dividers and Asynchronous Input Synchronization	—
Week 13	Nov 16–20	**Datapath and Control Architecture:** Connecting datapath execution units to sequential state controllers; microarchitectural trade-offs; FPGA Digital System Design Project due Friday. *Reading: Harris & Harris Ch. 7.1–7.3*	Lab 11: Single-Cycle Datapath Building Blocks and Register-ALU Integration	**FPGA Digital System Design Project due Fri Nov 20 at 11:59 p.m.**
Week 14	Nov 23	**FPGA Architecture and Implementation:** Configurable logic blocks (CLBs), lookup tables (LUTs), programmable interconnects, block RAM, and DSP slices on Xilinx Artix-7 devices. *Reading: Harris & Harris Ch. 5.7*	Lab 12: FPGA Implementation of Multi-Cycle Sequential Controller	*Nov 25–Nov 27: Thanksgiving break (no classes).*
Week 15	Nov 30–Dec 4	**Peripheral Interfaces and Communication Protocols:** Asynchronous serial communication (UART), SPI protocols, memory-mapped peripheral control, and hardware interface debugging. *Reading: Harris & Harris Ch. 8.1–8.3*	Lab 13: Serial Communication: UART Transmitter/ Receiver on FPGA	—
Week 16	Dec 7, 9	**Digital Hardware Verification and Course Review:** Boundary scan, built-in self-test (BIST), fault models, comprehensive semester review, and preparation for the final examination. *Reading: Review Harris & Harris Ch. 1–5, 7*	Lab 14: FPGA Capstone Project Demonstrations and Hardware Verification	*Wed Dec 9: Last day of classes. Thu Dec 10: Reading Day.*
Finals	Dec 14	**Comprehensive Final Examination:** Monday, December 14, 2026, 8:00–10:00 a.m., Rowan Engineering Center 110.	—	Comprehensive.

Course Policies

Attendance Policy

Regular attendance at both lecture and laboratory sessions is required to master digital logic design and hardware debugging. Laboratory sessions utilize specialized FPGA hardware and benchtop oscilloscopes that cannot be replicated outside scheduled hours. If an unavoidable absence arises due to illness or approved university events, notify Dr. Becker in advance. Students who miss the first two class meetings without notifying the instructor may be dropped. Students may miss class for religious observance without penalty if they notify the instructor in writing within the first two weeks of the semester (by Wednesday, September 9, 2026). Absences for university-sponsored activities (athletics, performances, conferences) are excused with a letter from the sponsoring office at least one week in advance.

Late Work Policy

Homework problem sets submitted after the deadline incur a 15% penalty per 24 hours late, up to 48 hours. Laboratory checkoffs must be completed during the scheduled lab session or within open lab hours prior to Sunday at 11:59 p.m.; late lab reports incur 10% per day. To accommodate personal emergencies, the lowest homework score and lowest lab score will be dropped.

Final Exam Policy

The final examination (Monday, December 14, 2026, 8:00–10:00 a.m.) is scheduled by the University Registrar and can't be moved without the Dean's written approval (Faculty Handbook §5.5). A student with

three or more final exams on the same calendar day may reschedule one of them. Requests go to the instructor of the middle exam by the last day of classes. For this term, send the request by Wednesday, December 9, 2026 (Student Handbook §6.4).

Academic Integrity

Alkimi University is an academic community devoted to rigorous scholarship, open intellectual inquiry, and uncompromising ethical conduct. All students are subject to the regulations of the Alkimi University Academic Integrity Policy. Academic dishonesty—including plagiarism, cheating on examinations, unauthorized collaboration, fabrication of empirical data, and unauthorized submission of academic work generated by artificial intelligence—undermines the integrity of the university and carries severe disciplinary sanctions. Sanctions range from a failing grade on an assignment or exam to an administrative course failure recorded as an 'XF' on the official transcript, academic suspension, or expulsion. Suspected violations are formally investigated and resolved through the Office of Academic Integrity in accordance with Faculty Handbook §6. For detailed information, consult the Office of Academic Integrity, Lovell Hall 315, (555) 555-0163, integrity@university.alkimi.ai.

Accessibility Services

Alkimi University is committed to providing equitable educational access and reasonable accommodations for all students with documented disabilities, including physical, sensory, psychological, learning, and chronic health conditions. Students requesting academic accommodations must formally register with the Office of Accessibility Services, Harlan Hall 204, (555) 555-0155, access@university.alkimi.ai. Once approved, students will receive an official Faculty Accommodation Letter detailing approved accommodations. Students should present this letter to the instructor as early in the semester as possible, and at least one week prior to any exam or assignment requiring accommodation. Accommodations cannot be applied retroactively.

Student Wellness and Mental Health

Your physical health, psychological well-being, and mental health are essential to your academic success. If you experience heightened stress, anxiety, depressive symptoms, personal trauma, or academic burnout, free, confidential counseling and medical care are available through the Hollis Health & Counseling Center, located in the Hollis Center. Routine appointments are available Monday–Friday 8:00 a.m.–6:00 p.m. and Saturday 10:00 a.m.–2:00 p.m. during the semester by calling (555) 555-0190 or emailing health@university.alkimi.ai. Urgent, 24/7 crisis psychological counseling is accessible immediately at (555) 555-0199.

Campus Student Support Services

- **Academic Advising Center:** Lovell Hall 101 | (555) 555-0158 | advising@university.alkimi.ai
- **Writing Center:** Whitcombe Library 3rd Floor | Free consultations on papers, reports, and research projects at any stage.
- **Whitcombe Library:** Whitcombe Library, Main Floor | (555) 555-0170 | askalibrarian@university.alkimi.ai
- **Hollis Health & Counseling Center:** Hollis Center | (555) 555-0190 | 24/7 Counseling Line: (555) 555-0199 | health@university.alkimi.ai
- **Digital Systems & FPGA Lab Help:** Rowan Engineering Center 150 | Open lab hours with teaching assistant support Monday and Wednesday 4:00–7:00 p.m.